DETAILED DESCRIPTION OF PACKAGES

A2.1 GENERAL

The package dimensions are 5 1/4" long + 0.3" for the printed plug spigot, 4.3" wide x 1/16" thick laminate clad with 0.0014" copper. Double-sided printed circuits are used, and 22 outlets are available from each side of the printed board. Socket pins are numbered in pairs from top to bottom, L or R being added to show contacts on the left or right respectively (seen from the rear).

Packages are inserted into the computer with components on the left (seen from the front) and the bevel on the front edge upwards. There are coded slots in the printed plug to avoid wrong insertions, and the monitor points are numbered from top to bottom.

A2.2 NOR PACKAGE

Figure 8 (B65/52701) is the circuit diagram of this package. There are six NOR circuits, two with three inputs, two with two inputs and two with only a single diode. (These last may be used directly as inverters). There are also four spare diodes, which may be connected to the common OR point (pins 12L, 13L, 10L, 17L, l6L) of a circuit on their own or another package.

The OR operation is performed by the diodes and inversion by the transistor, which is not directly connected to a load. Collectors and an associated load resistor are taken to opposing pins of the same number, so that in simple cases a strap is all that is needed. If common collector gating is used, then the appropriate

collectors are connected together and to one collector load. It is also possible to use multiple collector loads for speed compensation.

There are six monitor points at the front of the package, connected to the six collectors. The circuits are designed to work in an ambient temperature of 55°C. Detailed performance checks must be made using the test specification, but the edge delay through, two lightly loaded gates in series should never exceed 50 ns.

A2.3 SINGLE ENTRY FLIP-FLOP

Figure 9 (B65/52715) is the circuit diagram of this package. There are two identical circuits, each a single-entry diode-pump flip-flop or toggle. The 0 inputs are on pins 9R and 14L, the 1 inputs on 8R and 13R. The shift pulse connection is made to 7L or 9L for the top circuit and 17L or 20L for the bottom circuit. The 0 outputs are on 12L and 13L (top) and 15L and 16L (bottom) the corresponding 1 outputs being on pins 5R and 6R, l8R and 19R. Each collector is taken to a monitor point, the 1 outputs are taken through 100K ohm to pins 11R and 22R for connection to DM160 fluorescent indicators. An indicator connection is also taken through 6.8K ohm resistors to pins 8L and l8L for monitoring without disturbing circuit conditions.

C_4, C_2, C_8 and C_6 are the pump capacitors, D_4, D_1, D_{10} and D_7 the corresponding diodes to the transistor bases. C_9 and L_1 decouple the -6V rail from the circuit and vice versa. The circuit is designed to function up to a temperature of 55°C. Detailed performance checks should be made using the test specification, but

the circuits should switch within 100 ns of the application of a rapid pulse.

A2.4 TRIPLE-ENTRY FLIP-FLOP PACKAGE

Figure 11 (B65/52704) is the circuit diagram of this package. There is one circuit only on the package, which is similar to the single entry flip-flop or toggle with two extra diode pump inputs.

The 0 inputs are on pins 7R, 6R and 5R, corresponding 1 inputs appearing on 20L, 21L and 22L. The shift pulses in the same order are on pins 9L, 8L and 16L. The 0 output is on pins 14L and 15L, the 1 output on pins 10L and 11L with 100K ohms to 13L for a DM 160 fluorescent indicator.

C_2, C_3, C_4, C_8, C_7 and C_6 are the pump capacitors, D_1, D_4, D_7, D_{16}, D_{13} and D_{10} are the corresponding diodes connected to the transistor bases. C_9 and L_1 decouple the -6V rail from the circuit and vice versa.

The circuit is designed to operate up to 55°C. Detailed performance checks should be made using the test specifications, but the circuit should switch within 100ns of the application of a rapid pulse.

A2.5 POWER NOR PACKAGE

Figure 12 (B65/52783) is the circuit diagram of the power NOR package. The connection details are identical in every way to those for the simple NOR (section 2).

The OR operation is performed by diodes, as. before, but these drive an ASZ 21 emitter follower before the inversion by a 2N985 transistor connected for common emitter operation.

The circuits are designed to work in an ambient temperature of 55°C. Detailed performance checks should be made using the test specification, but the edge delay through two lightly loaded gates should never exceed 60 ns.

A2.6 PULSE GATE PACKAGE

Figure 10 (B65/52782) is the circuit diagram for this package. There are three identical circuits on the package, each one taking a digit input (9R, 10L, 13L, 14L, 15L) and each capable of having extra diodes added at 10R, 11L and 21L.

A positive pulse drive to each circuit is taken from pins 11R, 17R and 22L through a differentiating capacitor C_1, C_3 and C_5 which enables edges to be used. If the input is held near earth, then the pulse input is amplified by the circuit and drives the set of five output pins (12R 13R 14R 15R l6R, l8R 19R 20R 21R 22R, l6L 17L l8L 19L 20L) from the low impedance of a complementary pair of emitter followers.

C_7 and L_1 decouple the main -6V rail, a variable -6V rail may be used on pin 2L for testing margins. Each output is taken to a monitor point through 220 ohms.

The circuit is designed to operate up to 55°C ambient temperature. Detailed performance checks should be made using the test specification.